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e. a second plurality of registers coupled to receive the plurality of activation signals, wherein each register of the second plurality contains a vector address for the corresponding activation signal, the second plurality of registers for providing to the microprocessor the vector address corresponding to the highest priority enabled activation signal.

10. The apparatus according to claim 9 wherein the priority encoding circuit comprises a plurality of logical AND gates, each logical AND gate corresponding to one of the activation signals other than a highest priority of the activation signals, wherein each logical AND gate is coupled to perform a logical AND function on a logic level of the corresponding one of the activation signals and on an inverted logic level of each activation signal having a priority higher than the corresponding one of the activation signals and wherein an output of each logical AND gate and the highest priority of the activation signals are each coupled to enable a corresponding one of the second plurality of registers to provide its vector address to the microprocessor.

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11. The apparatus according to claim 9 wherein relative priorities of the interrupt signals are altered by altering the contents of the first and second plurality of registers.

12. The apparatus according to claim 9 wherein selected ones of the plurality of interrupts are masked by appropriately configuring the contents of the respective one of the first plurality of registers.

13. The apparatus according to claim 9 wherein selected ones of the plurality of interrupts are masked by appropriately configuring the contents of the respective one of the first plurality of registers to select an output of the corresponding de-multiplexer which is not connected to one of the plurality of logical OR gates.

14. The apparatus according to claim 9 wherein one vector address corresponds to more than one interrupt signal.

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