register **212** is the highest priority and the interrupt mapped to the vector address register **202** is the lowest priority. Accordingly, whenever an interrupt signal mapped to the output of the logical "OR" gate **320** (in the example, the interrupt signal INT. C) is active, the output of the logical "OR" gate **320** will block all the other interrupt signals via the logical "AND" gates **322–328** and will cause the vector address contained in the register **212** (in the example, the vector address C') to be placed on the vector address bus **330**.

Assuming none of the higher priority interrupt signals are active, whenever an interrupt signal mapped to one of the outputs of the "OR" gates **312–318** is active, the output of the "OR" respective "OR" gate will block all the lower priority interrupt signals via the logical "AND" gates associated with the lower priority interrupt signals and will cause the vector address corresponding to the highest priority active interrupt signal to be placed on the vector address bus **330**.

Once the highest priority interrupt has been serviced by executing the appropriate interrupt service routine, the interrupt signal is disabled and the next highest priority pending interrupt is serviced until there are no more pending interrupts. Once there are no pending interrupts, the program counter is restored such that the microprocessor resumes executing the software program.

Therefore, according to the present invention, the interrupt signals are configurable according to the contents of the of the plurality of interrupt configuration registers **102–110** and according to the contents of the vector address registers **202–212**. These contents are relatively easily changed, thus, the present invention provides more readily configurable interrupts in comparison to prior techniques.

The present invention has been described in terms of specific embodiments incorporating details to facilitate the understanding of the principles of construction and operation of the invention. Such reference herein to specific embodiments and details thereof is not intended to limit the scope of the claims appended hereto. It will be apparent to those skilled in the art that modifications may be made in the embodiment chosen for illustration without departing from the spirit and scope of the invention. Specifically, it will be apparent to one of ordinary skill in the art that the device of the present invention could be implemented in several different ways and the apparatus disclosed above is only illustrative of the preferred embodiment of the invention and is in no way a limitation. For example, it will be apparent that modifications or additions can be made to the apparatus illustrated in FIG. **3**. In particular, logic circuits can be included which latch the interrupt signals INT. A, INT. B, INT. C, INT. D and INT. E and which control whether each interrupt signal is leading edge, trailing edge or level sensitive. Further, alternate techniques for masking the interrupts can be implemented, such as by selectively controlling a chip select pin for each of the de-multiplexers **302**, **304**, **306**, **308** and **310**.

What is claimed is:

1. A method for responding to active ones of a plurality of interrupt signals in a microprocessor-based system, the method comprising the steps of:

a. receiving the active ones of the plurality of interrupt signals;

b. mapping each of the active ones of the plurality of interrupt signals, according to contents of a respective one of a first plurality of registers, to one of a second plurality of registers, wherein each register of the second plurality has a corresponding relative priority specified by the respective one of the first plurality of registers and contains a vector address for the corresponding interrupt signal; and

c. supplying the vector address for each of the active ones of the interrupt signals to the microprocessor according to the relative priority of each of the active ones of the interrupt signals.

2. The method according to claim **1** further comprising a step of altering relative priorities of the interrupt signals by altering the contents of the first and second plurality of registers.

3. The method according to claim **1** further comprising a step of masking a selected one of the plurality of interrupts according to the contents of the respective one of the first plurality of registers.

4. The method according to claim **1** wherein one vector address corresponds to more than one interrupt signal.

5. An apparatus for responding to active ones of a plurality of interrupt signals in a microprocessor-based system, the apparatus comprising:

a. a first plurality of registers;

b. a mapping circuit coupled to the first plurality of registers for mapping each of the active ones of the plurality of interrupt signals to a plurality of activation signals based on priority according to contents of a respective one of a first plurality of registers;

c. a priority encoding circuit coupled to the mapping circuit for blocking all but a highest priority activation signal of the plurality of activation signals; and

d. a second plurality of registers coupled to receive the plurality of activation signals, wherein each register of the second plurality contains a vector address for the corresponding activation signal, the second plurality of registers for providing to the microprocessor the vector address corresponding to the highest priority activation signal.

6. The apparatus according to claim **5** wherein relative priorities of the interrupt signals are altered by altering the contents of the first and second plurality of registers.

7. The apparatus according to claim **5** wherein selected ones of the plurality of interrupts are masked by the mapping circuit according to the contents of the respective one of the first plurality of registers.

8. The apparatus according to claim **5** wherein one vector address corresponds to more than one interrupt signal.

9. An apparatus for responding to active ones of a plurality of interrupt signals in a microprocessor-based system, the apparatus comprising:

a. a first plurality of registers for storing a relative priority value, each register of the first plurality corresponding to one of the plurality of interrupt signals;

b. a plurality of de-multiplexers, each de-multiplexer having a plurality of select lines coupled to a respective one of the first plurality of registers to receive the relative priority value, an input coupled to receive the corresponding one of the interrupt signals, and a plurality of outputs;

c. a plurality of logical OR gates, each logical OR gate having a plurality of inputs and an output, wherein each input of each logical OR gate is coupled to one of the plurality of outputs of each de-multiplexer, wherein the outputs of the logical OR gates form a plurality of activation signals;

d. a priority encoding circuit coupled to the plurality of OR gates for blocking all but a highest priority enabled activation signal of the plurality of activation signals; and