de-multiplexers are combined with corresponding outputs of each other de-multiplexer according to the logical "OR" function by a plurality of logical "OR" gates to provide a plurality of activation signals at the outputs of the logical "OR" gates. Each activation signal is selectively enabled according to a condition of the corresponding interrupt signal. Thus, the de-multiplexers and logical "OR" gates map the interrupt signals to the outputs of the logical "OR" gates according to the contents of the interrupt configuration registers.

Each activation signal corresponds to one of the plurality of vector address registers. A plurality of logical "AND" gates are coupled to receive the activation signals and to allow only the highest priority enabled activation signal to enable the corresponding one of the plurality of vector address registers. The vector address stored in the enabled vector address register is placed on a vector address bus for the microprocessor. The microprocessor then places the vector address in its program counter and executes the appropriate interrupt service routine beginning at the vector address.

Once the highest priority interrupt has been serviced by executing the appropriate interrupt service routine, a next highest priority pending interrupt is serviced until there are no more pending interrupts. Once there are no pending interrupts, the program counter is restored such that the microprocessor resumes executing its original sequence of instructions.

Therefore, according to the present invention, the interrupts are configurable according to the contents of the plurality of interrupt configuration registers and according to the contents of the vector address registers. These contents are relatively easily changed, thus, the present invention provides more readily configurable interrupts in comparison to prior techniques. In addition, the present invention reduces latency in servicing each interrupt by eliminating priority and vector address parsing in an interrupt handler as required prior techniques. Rather, prioritizing each interrupt and providing the appropriate vector address for the interrupt is performed according to the present invention primarily in hardware, resulting in less latency than in prior techniques.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a functional block diagram according to the present invention including a plurality of interrupt configuration registers and a plurality of vector address registers.

FIGS. **2**A–D illustrate examples for assigning priorities and mapping vector addresses to interrupts according to the present invention.

FIG. **3** illustrates a schematic diagram of a circuit for implementing the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Referring to FIG. **1**, a plurality of interrupt configuration registers **100** and a plurality of vector address registers **200** are provided for responding to interrupt signals in a microprocessor-based system. Each interrupt signal INT. A through INT. n generated by a peripheral device corresponds to one of the plurality of interrupt configuration registers **100**. The number of interrupt signals varies depending upon the system implementation. Each of the interrupt configuration registers **100** is configurable by software to include a bit pattern that identifies one of the vector address registers **200** or a bit pattern that indicates that the corresponding interrupt is to be masked (disabled). Accordingly, the interrupt signals INT. A through INT. n are each selectively mapped to an appropriate one of the registers **200** according to the contents of the registers **100**.

Each of the plurality of vector address registers **200** contains the starting address of an interrupt service routine appropriate for the corresponding interrupt signal. In a system that utilizes 32 bits to specify memory addresses, each of the registers **200** holds 32 bits, though it will be apparent that for other addressing schemes, the registers **200** can have another size. The vector address registers **200** are arranged according to a predetermined priority. For example, the vector address register **202** is designated the lowest priority, intermediate registers, such as the register **204**, having ascending priority levels while the vector address register **206** is designated the highest priority level. It will be apparent, however, that the relative ordering of priorities can be altered.

The number of bits stored by each of the interrupt configuration registers **100** is preferably sufficient to provide a unique bit pattern for each of the vector address registers **200** and to provide a unique bit pattern to indicate a masked interrupt. Thus, if there are up to three interrupt signals, each of the registers **100** preferably hold two bits. One bit pattern, such as 00, indicates that the corresponding interrupt is masked, while the remaining bit patterns 01, 10 and 11, each correspond to one of the vector address registers **200**. If there are up to seven interrupt signals, the plurality of interrupt configuration registers **100** preferably each hold three bits. One bit pattern, such as 000, indicates that the corresponding interrupt is masked. Each of the remaining bit patterns, 001 to 111, corresponds to one of the vector address registers **200**. Alternately, if there are up to fifteen interrupt signals, each of the plurality of configuration registers preferably holds four bits. It will be apparent that in a system having even more interrupts, more bits are needed.

The following examples illustrate operation of the present invention. Assume a microprocessor-based system must respond to five different interrupt signals designated INT. A through INT. E. Thus, there must be five interrupt configuration registers **100**, each of which stores three bits. In addition, there must be five vector addresses, designated A' through E'. For the following examples, the vector addresses A' through E' each correspond to an interrupt having a like letter designation (e.g. the interrupt service routine appropriate for the INT. A has a starting address in memory of Address A').

A first example is illustrated in FIG. **2**A. Assume it is desired to assign priorities to the interrupts A through E in the following order (highest priority to lowest priority): C, E, A, D, B. Therefore, the interrupt configuration registers **100** and vector address registers **200** are configured as illustrated in FIG. **2**A: the bit pattern **101** is placed in the interrupt configuration register corresponding to the interrupt INT. C, indicating that INT. C is to be mapped to the highest priority of the vector address registers **200**, while the vector address C' for INT. C is placed in the highest priority vector address register; the bit pattern **100** is placed in the interrupt configuration register corresponding to the interrupt INT. E, indicating that INT. E is to be mapped to the second highest priority of the vector address registers **200**, while the vector address E' for INT. E is placed in the second highest priority vector address register; the bit pattern 011 is placed in the interrupt configuration register corresponding to the interrupt INT. A, indicating that INT. A is to be