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[54] SOFTWARE CONFIGURABLE TECHNIQUE FOR PRIORITIZING INTERRUPTS IN A MICROPROCESSOR-BASED SYSTEM

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[57] ABSTRACT

A software configurable technique for prioritizing and masking interrupts in a microprocessor-based system. Contents of a first plurality of registers map each of a plurality of interrupts to an appropriate one of a second plurality of registers and indicate which interrupts are masked. The second plurality of registers are arranged in a predetermined priority and each contains the starting address of an appropriate interrupt service routine for the corresponding interrupt. The interrupt signals are mapped to the outputs of a plurality of logical "OR" gates according to the contents of the first plurality of registers by a plurality of de-multiplexers coupled to the inputs of the plurality of logical "OR" gates. Each logical "OR" gate corresponds to one of the second plurality of registers. A plurality of logical "AND" gates are coupled to the outputs of the logical "OR" gates so as to allow only the highest priority enabled interrupt signal to enable the corresponding one of the second plurality of registers. The vector address stored in the enabled register is placed on a vector address bus for the microprocessor which places the vector address in its program counter. The microprocessor is then interrupted and begins executing the appropriate interrupt service routine beginning at the appropriate vector address. The present invention provides readily configurable interrupts by altering the contents of the first and second plurality of registers.

14 Claims, 7 Drawing Sheets

