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[54] TESTING OF HARDWARE BY USING A HARDWARE SYSTEM ENVIRONMENT THAT MIMICS A VIRTUAL SYSTEM ENVIRONMENT

[75] Inventors: **Steven R. Cox**, San Jose; **Harry M. Chue**, Alameda, both of Calif.

[73] Assignees: **Sony Corporation**, Tokyo, Japan; **Sony Electronics Inc.**, Park Ridge, N.J.

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[58] **Field of Search** 395/500; 364/578

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Primary Examiner—Kevin J. Teska
Assistant Examiner—Samuel Broda
Attorney, Agent, or Firm—Haverstock & Owens LLP

[57] **ABSTRACT**

A technique for testing a hardware implementation of an integrated circuit design using test algorithms developed for testing a software model of the integrated circuit design. A software model is created for a design of the integrated circuit. The software model is a software algorithm that emulates behavior of the integrated circuit. In addition, a virtual environment for the software model is also constructed. The virtual environment is a software algorithm that emulates an actual environment anticipated for the integrated circuit. Diagnostic tests are performed on the software model while it is operating in the virtual environment. These tests are used to verify and analyze the design for the integrated circuit. Based upon the results of the diagnostic tests, the design is modified as necessary. Once the design for the integrated circuit has been verified by testing the software model, an actual hardware circuit is constructed that implements the software model. In addition, an actual hardware environment is constructed that implements the virtual environment. Accordingly, the software model and the virtual environment are transformed into equivalent hardware circuits. Because of the equivalency between the software model and the hardware circuit and between the virtual environment with the hardware environment, the same diagnostic tests that were used to verify and analyze the software model in the virtual environment can be used to verify and analyze the hardware circuit in the hardware environment. This results in good test coverage for the integrated circuit design and reduced expense for developing the diagnostic tests.

11 Claims, 3 Drawing Sheets